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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application No.	10/676,310
Filing Date	September 30, 2003
First Named Inventor	Stephan Jourdan
Art Unit	2183
Examiner Name	Brian P. Johnson
Total Number of Pages in This Submission	22
Attorney Docket Number	42P17034

ENCLOSURES *(check all that apply)*

- [X] Fee Transmittal Form
  - [X] Fee Attached
- [ ] Amendment / Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
  - [ ] PTO/SB/08
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Basic Filing Fee
  - [ ] Declaration/POA
- [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s)
  - [ ] Landscape Table on CD
- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [X] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm *or* Individual name	Angelo J. Gaz, Reg. No. 45,907 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	
Date	11/6/06

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I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Typed or printed name	Suzanne Johnston		
Signature		Date	11/6/06

FEE TRANSMITTAL for FY 2005

Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT	($)	500.00

Complete if Known	
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METHOD OF PAYMENT *(check all that apply)*

☒ Check ☐ Credit card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 02-2666 Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below
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FEE CALCULATION

1. EXTRA CLAIM FEES

			Extra Claims		Fee from below		Fee Paid
Total Claims	22	- 22** =	0	X	50.00	=	$0.00
Independent Claims	3	- 3** =	0	X	200.00	=	$0.00
Multiple Dependent						=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	50	2202	25	Claims in excess of 20
1201	200	2201	100	Independent claims in excess of 3
1203	360	2203	180	Multiple Dependent claim, if not paid
1204	790	2204	395	**Reissue independent claims over original patent
1205	300	2205	150	**Reissue claims in excess of 20 and over original patent

**or number previously paid, if greater, For Reissues, see below

SUBTOTAL (1) ($) 0.00

2. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
2053	130	2053	130	Non-English specification	
1251	120	2251	60	Extension for reply within first month	
1252	450	2252	225	Extension for reply within second month	
1253	1,020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	500.00
1403	1,000	2403	500	Request for oral hearing	
1451	1,510	2451	1,510	Petition to institute a public use proceeding	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
1809	790	1809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	
Other fee (specify)					

SUBTOTAL (2) ($) 500.00

SUBMITTED BY

Complete (if applicable)

Name (Print/Type)	Angelo J. Gaz	Registration No. (Attorney/Agent)	45,907	Telephone	(310) 207-3800
Signature				Date	11/6/06

Based on PTO/SB/17 (12-04) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 12/15/2004.
SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

PATENT
Attorney's Docket No. 42P17034

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application for:	Examiner: Brian P. Johnson
Stephan Jourdan, et al.	Art Unit: 2183
Serial No.: 10/676,310	Confirmation No.: 8184
Filed: September 30, 2003	
For: **DETERMINATION OF WHETHER ONE OR MORE MICRO OPERATIONS BELONG TO A BRANCH PATH THAT IS DEPENDENT ON A MISPREDICTED BRANCH BASED ON ASSIGNED IDENTIFICATION**	

APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicant (hereinafter "Appellant") submits one copy of the following Appeal Brief pursuant to 37 C.F.R. § 1.192 for consideration by the Board of Patent Appeals and Interferences. Attached please find a check for $500.00 to cover the cost of filing the opening brief as required by 37 C.F.R. § 41.20(b)(2). Please charge any additional amount due or credit any overpayment to deposit Account No. 02-2666.

11/09/2006 ZJUHAR1 00000043 10676310
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I. REAL PARTY IN INTEREST

Stephan Jourdan, Per Hammarlund, Avinash Sodani, James Allen, Francis McKeen, and Pierre Michaud, the parties named in the caption, transferred their rights in the subject application "Determination of Whether One or More Micro Operations Belong to a Branch Path that is Dependent on a Mispredicted Branch Based on Assigned Identification" to Intel Corporation of Santa Clara, California. Thus, as the owner at the time the brief is being filed, Intel Corporation of Santa Clara, California is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences that will directly affect or be directly affected by or have a bearing on the Board's decision in this Appeal.

III. STATUS OF CLAIMS

Claims 1-22 are pending and rejected in this application. Claims 1-22 are appealed herein.

IV. STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Final Office Action.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Three independent claims (claims 1, 10 and 19) are presented in this appeal.

Independent claim 1 describes a method comprising:

assigning an identification number (ID) to each of a plurality of micro-operations (uops) to identify a branch path to which the uop belongs; (see Appellant's specification assigning (block 300 of Figure 3 and paragraph 29) an identification number to each of a plurality of micro-operations to identify a branch path to which the micro-operation belongs (branch identification 202 of Figure 2 and paragraphs 11 and 15), without limitation thereto)

determining whether one or more branches are predicted correctly; (see Appellant's specification determining (block 302 Figure 3 and paragraph 29) whether one or more branches are predicted correctly (see paragraph 13), without limitation thereto)

determining which of the one or more branch paths are dependent on a mispredicted branch; and (see Appellant's specification determining (block 303 of Figure 3 and paragraph 29) which of the one or more branch paths are dependent on a mispredicted branch (paragraphs 14-16), without limitation thereto)

determining whether one or more of the plurality of uops belong to a branch path that is dependent on the mispredicted branch based on their assigned IDs. (see Appellant's specification determining (block 306 Figure 3 and paragraph 29) whether one or more of the plurality of uops belong to a branch path that is dependent on the mispredicted branch based on their assigned IDs (paragraphs 14-16), without limitation thereto)

Independent claim 10 describes an apparatus comprising:

an allocator to assign a plurality of micro-operations (uops) identification numbers (IDs), each ID to identify a branch path to which the uop belongs; (see Appellant's specification an allocator (allocator 102, Figure 1, paragraphs 11-12) to assign a plurality of micro-operations (uops) identification numbers, each ID to identify a branch path to which the uop belongs (see block 300 of Figure 3, branch ID 202 of Figure 2, and paragraphs 11, 15 and 29), without limitation thereto)

a jump unit coupled to the allocator to determine whether branches are predicted correctly; and (see Appellant's specification jump unit (jump unit 104 of Figure 1 and paragraphs 11 and 13-14) coupled to the allocator to determine whether branches are predicted correctly (see block 302 of Figure 3 and paragraphs 13 and 29) without limitation thereto)

an execution unit coupled to the jump unit to determine which uops belong to a branch path that is dependent on a mispredicted branch based on their assigned IDs. (see Appellant's specification execution unit (execution unit 106 of Figure 1 and paragraph 11) coupled to the jump unit to determine which uops belong to a branch

path that is dependent on a mispredicted branch based on their assigned IDs (block 306 of Figure 3, paragraph 14-16 and paragraph 29), without limitation thereto)

Independent claim 19 describes a system comprising:

an input/output (I/O) controller; and (see Appellant's specification I/O controller 416 of Figure 4 and paragraph 30, without limitation thereto)

a processor coupled to the I/O controller, the processor including: (see Appellant's specification processor 402 of Figure 4 and paragraph 30, without limitation thereto)

an allocator to assign micro-operations (uops) identification numbers (IDs), each ID to identify a branch path to which the uop belongs; (see Appellant's specification an allocator (allocator 102, Figure 1, paragraphs 11-12) to assign micro-operations (uops) identification numbers, each ID to identify a branch path to which the uop belongs (see block 300 of Figure 3, branch ID 202 of Figure 2, and paragraphs 11, 15 and 29), without limitation thereto)

a jump unit coupled to the allocator to determine whether branches are predicted correctly; and (see Appellant's specification jump unit (jump unit 104 of Figure 1 and paragraphs 11 and 13-14) coupled to the allocator to determine whether branches are predicted correctly (see block 302 Figure 3 and paragraphs 13 and 29) without limitation thereto)

an execution unit coupled to the jump unit to determine which uops belong to a branch path that is dependent on a mispredicted branch based on their assigned IDs. (see Appellant's specification execution unit (execution unit 106 of Figure 1 and paragraph 11) coupled to the jump unit to determine which uops belong to a branch path that is dependent on a mispredicted branch based on their assigned IDs (block 306 of Figure 3, paragraph 14-16 and paragraph 29), without limitation thereto)

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The grounds of rejection involved in this appeal are as follows:

Claims 1-2, 6-13 and 17-22 are rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,065,115 to Sharangpani et al. (Sharangpani).

Claims 3-5 and 14-16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Sharangpani in view of U.S. Patent Application Publication No. 2003/0061258 to Rodgers et al. (Rodgers).

VII. ARGUMENT

A. Overview of the Prior Art

1. Overview of Sharangpani

Sharangpani discloses storing a tag that associates an instruction stream with a particular instruction pointer (see Figure 5 tag 504). In order to find out which branch path is associated with an instruction, it is necessary that the instruction is associated with a particular stream, the stream is associated with an instruction pointer, and the instruction pointer is associated with a target instruction stream (see col. 10, lines 6-20). It is a principle of operation of Sharangpani to use tag field 504 to ensure proper concurrent execution of multiple instruction streams (see col. 10, lines 21-32), to use stream table 330 to ensure proper instruction retirement processing (see col. 10, lines 33-39) and to use stream table 330 to ensure that all instructions are retired in a correct order to ensure proper processing functionality (see col. 6, lines 5-14 and col. 11 lines 48-67). Notably, Sharangpani teaches satisfying this principle of operation using tag field 504 to store a simple tag identifying one instruction stream for each instruction pointer number 502 (see Figure 5 and col. 10, lines 6-10), but does not need to assign to each micro-operation a number identifying which stream that operation belongs to (see Figure 5 and cancellation of an instruction stream associated with an instruction pointer at col. 10, lines 33-39)..

2. Overview of Rodgers

Rodgers teaches a principle of operation of multi-threading by limiting a first set of read and write pointers to the first predetermined number of entries; limiting a second set of read and write pointers to a second predetermined number of entries; and providing in instruction streaming buffer 106, trace cache 62 and instruction queue 103, a logically partitioned storage capacity between the first and second threads (see paragraph 60). Rodgers also discloses assigning a sequence number to each microinstruction to track the logical order within a thread where the instructions are indexed within reorder table 180 by sequence number in a sequential and in-order manner (see paragraph 64 and 80), but does not need to assign an identification number to each micro-operation to identify a branch path to which the micro-operation belongs.

B. Rejection of Claims 1-2, 6-13 and 17-22 Under 35 U.S.C. § 102(b)

The Patent Office rejects claims 1-2, 6-13 and 17-22 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,065,115 to Sharangpani et al. (Sharangpani).

1. Claims 1-2 and 6-9

Appellant respectfully disagrees with the rejection above and submit that claims 1-2 and 6-9 (e.g., as claims 2 and 6-9 depend form claim 1) are allowable for at least the reason that Sharangpani does not disclose "assigning an identification number (ID) to each of a plurality of micro-operations (uops) to identify a branch path to which the uop belongs" as required by independent claim 1.

Identifying

Sharangpani discloses storing a tag that associates an instruction stream with a particular instruction pointer instead of "identifying a branch path to which the uop belongs." This difference is best demonstrated by carefully considering how efficiently an instruction can be associated with a branch path. According to the cited language of claim 1, the branch path of a particular instruction can be found by simply looking at the tag for the instruction. However, in Sharangpani additional steps are required to find out which branch path is associated with an instruction. First, the instruction is associated with a particular stream. Second, the stream is associated with an instruction pointer. Third, the instruction pointer is associated with a target instruction stream (See

Sharangpani, col. 10, ll. 6-20). Therefore, in Sharangpani, at least the extra steps of determining which instruction stream is associated with the instruction pointer and associating the instruction pointer with the target instruction are necessary to associate the individual instructions of the stream with their respective branch path. The extra steps necessary to identify the branch path associated with the instruction highlights the difference between the tag in Sharangpani and the ID in the claim.

In contrast, Appellant's identification tag identifies a branch path to which the uop belongs, thereby reducing the number of steps needed to identify the branch path to which the uop belongs. Thus, the fact that the association can be performed in fewer steps than in Sharangpani illustrates that the cited claim language is different from the cited passages of Sharangpani. Moreover, according to claim 1, for example, as is shown in Figures 2 and 3 and described at paragraphs 11-16 of the application without limitation thereto, by assigning a branch path identification number to each micro-operation, each operation can also be assigned a branch unique sequence number. Thus, upon determination of a mispredicted branch, a table containing the branch identification numbers and sequence numbers can be quickly indexed to find which specific micro-operation was the last valid operation so that each subsequent operation of that branch can be invalidated, as an operation belonging to the mispredicted branch. It can be appreciated that invalidating any instruction that has a sequence number greater than the oldest valid instruction in the same branch will be performed much quicker by indexing by branch ID a table including a branch ID assigned to each instruction, than it would by using the three-step process of Sharangpani to determine to which branch each instruction belongs (e.g., see paragraph 14 of the application). In addition, by assigning a branch ID per instruction, if a branch was mispredicted, instructions for the correct branch can each be assigned a different/new branch identification so that they can begin to be decoded and allocated even while the previous, mispredicted instructions still exist in various units of the microprocessor (see paragraph 13 of the application). Again, as each of these instructions is assigned a new and different branch identification, it is more efficient to distinguish the correct instructions from the mispredicted instructions by examining the branch ID, as compared to three-step process of Sharangpani. Hence, for at least the reason that Sharangpani does not disclose the "identifying a branch path to which the uop belongs"

limitation of claim 1, Appellants respectfully request the Board overturn the rejection above for claims 1-2 and 6-9.

2. Claims 10-13 and 17-18

In addition, Appellants also respectfully disagree with the rejection above and submit that claims 10-13 and 17-18 (e.g., as claims 11-13 and 17-18 depend from claim 10) are allowable for at least the reason that Sharangpani does not disclose an allocator to assign a plurality of micro-operations identification numbers, each ID to identify a branch path to which the micro-instruction belongs, as required by independent claim 10. An argument analogous to the one above for claim 1 applies for the allocator of claim 10 as well. Hence, for at least the reasons noted above for claim 1, the cited reference does not disclose the above-noted limitation of claim 10. Thus, Appellants respectfully request the Board overturn the rejection above of claims 10-13 and 17-18.

3. Claims 19-22

In addition, Appellants also respectfully disagree with the rejection above and submit that claims 19-22 (e.g., as claims 20-22 depend from claim 19) are allowable for at least the reason that Sharangpani does not disclose an allocator to assign a plurality of micro-operations identification numbers, each ID to identify a branch path to which the micro-instruction belongs, as required by independent claim 19. An argument analogous to the one above for claim 1 applies for the allocator of claim 19 as well. Hence, for at least the reasons noted above for claim 1, the cited reference does not disclose the above-noted limitation of claim 19. Thus, Appellants respectfully request the Board overturn the rejection above of claims 19-22.

C. Rejection of Claims 3-5 and 14-16 Under 35 U.S.C. § 103(a)

Claims 3-5 and 14-16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Sharangpani in view of U.S. Patent Application Publication No. 2003/0061258 to Rodgers et al. (Rodgers).

1. Claims 3-5

Appellants respectfully disagree with the rejection above and submit that claims 3-5 (e.g., as claims 3-5 depend from claim 1) are allowable for at least the reason that the

combination of Sharangpani and Rodgers is improper; and because the cited references do not teach or suggest "assigning an identification number (ID) to each of a plurality of micro-operations, each ID to identify a branch path to which the micro-operation belongs," as required by claim 1.

First, the rejection fails to provide a statutorily valid suggestion or motivation found in the art to modify Sharangpani in view of Rodgers. "[There] must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings." MPEP §2143. On pages 7 and 8, the Final Office Action states that:

> It would be desirable to have a system to ensure that all instructions are retired in a correct order to ensure proper processor functionality.
>
> It would have been obvious to one of ordinary skill in the art at the time of invention to have included Rodgers' issue/retire scheme of assigning and using sequence numbers in Sharangpani's processor for the benefit of ensuring proper operation.

"[For] the benefit of ensuring proper operation" is not proper motivation because it incorrectly assumes improper operation necessitating the incorporation of the Rodgers' issue/retirement scheme. However, Sharangpani discloses a way to "ensure that all instructions are retired in a correct order to ensure proper processor functionality" without being combined with Rodgers. (See Sharangpani, col. 6, ll. 5-14 and col. 11, ll. 48-67) Specifically, it is a principle of operation of Sharangpani to use tag field 504 to ensure proper concurrent execution of multiple instruction streams (see col. 10, lines 21-32), to use stream table 330 to ensure proper instruction retirement processing (see col. 10, lines 33-39), and to use stream table 330 to ensure that all instructions are retired in a correct order to ensure proper processing functionality (see col. 6, lines 5-14 and col. 11 lines 48-67). Notably, Sharangpani teaches satisfying this principle of operation using tag field 504 to store a simple tag identifying one instruction stream for each instruction pointer number 502 (see Figure 5 and col. 10, lines 6-10), but does not require, teach or suggest assigning to each micro-operation a number identifying which stream that operation belongs to. Instead, Sharangpani

teaches a principle of operation that requires the identification of a branch that each pointer is pointing to, but does not need to assign a branch number or sequence number to each instruction, instruction by instruction (see Figure 5 and cancellation of an instruction stream associated with an instruction pointer at col. 10, lines 33-39).

In order to ensure proper execution of multiple instruction streams, Rodgers teaches a principle of operation of multi-threading by limiting a first set of read and write pointers to the first predetermined number of entries; limiting a second set of read and write pointers to a second predetermined number of entries; and providing in instruction streaming buffer 106, trace cache 62 and instruction queue 103, a logically partitioned storage capacity between the first and second threads (see paragraph 60). Rodgers also discloses assigning a sequence number to each microinstruction to track the logical order within a thread where the instructions are indexed within reorder table 180 by sequence number in a sequential and in-order manner (see paragraph 64 and 80), but does not need to assign an identification number to each micro-operation to identify a branch path to which the micro-operation belongs. Thus, the principle of operation of Rodgers assigns sequence numbers to each instruction, but does not require a branch identification for each instruction, because it instead physically splits the branches between buffer 106, cache 62 and queue 103 (see paragraph 60). Hence, the Patent Office's attempt to "combine" references is not a combination of teachings but instead a substitution of one way of doing things with another, since both teachings are superfluous.

On the other hand, the current application teaches assignment of both a branch identification and a sequence number, per instruction, to allow correct branch instructions to be fetched, allocated, and decoded while mispredicted instructions are still in the microprocessor (see paragraph 13 of the specification); and to allow jump unit 104 to update the oldest valid instruction of the current branch and to more efficiently determine which branch identifications are invalid or dependent upon the mispredicted branch (see paragraphs 14 and 16 of the application). These functionalities resulting from using both numbers are not possible or contemplated according to the teachings of Sharangpani (which does not assign branch or sequence numbers to each instruction), Rodgers (compare jump unit 104 of Figure 1 of the

application with Figure 1 of Rodgers which excludes a jump unit), or the combination (as neither reference provides a motivation for such functionalities).

Thus, one of ordinary skill in the art would not be motivated to combine Sharangpani with Rodgers to provide the limitations of claim 1 because the principle of operation of each reference prohibits such a combination, without substituting one principle of operation for the other. In other words, there would be no additional "benefit" of proper processor functionality or proper operation from making the combination. Therefore, the cited motivation to combine fails to provide a proper suggestion or motivation found in the art to make the combination or modification. Rather, the combination seems to be based solely on hindsight after reviewing the Appellants' application. For at the reason that the combination of references is improper, Appellants respectfully request the Board overturn the rejection above for claims 3-5.

Second, Appellants disagree with the rejection above and submit that claims 3-5 (e.g., as claims 3-5 depend from claim 1) are allowable for at least the reasons that the cited references do not teach or suggest "assigning an identification number to each of the micro-operations," as required by claim 1. As discussed above, with regard to claims 1, 10, and 19, Sharangpani fails to teach "assigning an identification number (ID) to each of a plurality of micro-operations." Furthermore, Rodgers fails to cure this deficiency. Rodgers teaches a principle of operation of multi-threading by limiting a first set of read and write pointers to the first predetermined number of entries; limiting a second set of read and write pointers to a second predetermined number of entries; and providing in instruction streaming buffer 106, trace cache 62 and instruction queue 103, a logically partitioned storage capacity between the first and second threads (see paragraph 60). Rodgers also discloses assigning a sequence number to each microinstruction to track the logical order within a thread where the instructions are indexed within reorder table 180 by sequence number in a sequential and in-order manner (see paragraph 64 and 80), but does not need to assign an identification number to each micro-operation to identify a branch path to which the micro-operation belongs. Thus, Rodgers does not disclose or suggest "assigning an identification number to each of the micro-operations," as required by claim 1. Hence, the Patent Office has not identified and Appellants are unable to find any teaching or suggestion of the above-

noted limitation of claim 1 in Rodgers. Thus, for at least the additional reason that neither Sharangpani, Rodgers, nor the combination teaches or suggests the above-noted limitation of claim 1, Appellants respectfully request that the Board overturn the rejection above for claims 3-5.

2. Dependent Claims 14-16

Appellants respectfully disagree with the rejection above and submit that claims 14-16 (e.g., as claims 14-16 depend from claim 10) are allowable for at least the reason that the references cannot be properly combined; and the references do not teach or suggest assigning an identification number to each of a plurality of micro-operations, each ID to identify a branch path to which the micro-operation belongs, as required by claim 10. An argument analogous to the one above for claims 3-5 applies here as well. Hence, for at least those reasons, Appellants respectfully request the Board overturn the rejection above for claims 14-16.

CONCLUSION

Hence, Appellants respectfully request the Board overturn the rejection of claims 1-22 as being unpatentable, for at least the reasons noted above.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Dated: 11/6/06 By: _____
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_____ 11/6/06
Suzanne Johnston Date

VIII. CLAIMS APPENDIX

The claims involved in this Appeal are as follows:

1. (Original) A method comprising:

assigning an identification number (ID) to each of a plurality of micro-operations (uops) to identify a branch path to which the uop belongs;

determining whether one or more branches are predicted correctly;

determining which of the one or more branch paths are dependent on a mispredicted branch; and

determining whether one or more of the plurality of uops belong to a branch path that is dependent on the mispredicted branch based on their assigned IDs.

2. (Previously Presented) The method of claim 1, further comprising retiring a uop that belongs to the branch path dependent on the mispredicted branch.

3. (Original) The method of claim 1, further comprising assigning each of the plurality of uops a sequence number.

4. (Original) The method of claim 3, further comprising storing the sequence number of an oldest valid uop in each branch path.

5. (Original) The method of claim 4, further comprising comparing the sequence number of a uop to the sequence number of the oldest valid uop in a same branch path.

6. (Original) The method of claim 1, further comprising maintaining a list of available IDs.

7. (Original) The method of claim 6, wherein assigning an ID to each of a plurality of uops to identify a branch path to which the uop belongs comprises assigning by an allocator an ID for each of the plurality of uops from the list of available IDs.

8. (Original) The method of claim 7, further comprising stalling the allocator if there is no available ID to be assigned.

9. (Original) The method of claim 7, further comprising placing an ID on the list of available IDs when all uops that have been assigned that ID have been retired.

10. (Original) An apparatus comprising:

an allocator to assign a plurality of micro-operations (uops) identification numbers (IDs), each ID to identify a branch path to which the uop belongs;

a jump unit coupled to the allocator to determine whether branches are predicted correctly; and

an execution unit coupled to the jump unit to determine which uops belong to a branch path that is dependent on a mispredicted branch based on their assigned IDs.

11. (Previously Presented) The apparatus of claim 10, further comprising a retire unit coupled to the jump unit to retire uops that are related to the mispredicted branch.

12. (Previously Presented) The apparatus of claim 11, wherein the allocator is to further maintain a list of available IDs and assign an ID for each branch from the list of available IDs.

13. (Previously Presented) The apparatus of claim 12, wherein the retire unit is to further place an ID on the list of available IDs when all uops that have been assigned that ID have been retired.

14. (Previously Presented) The apparatus of claim 10, wherein the allocator is to further assign each of the plurality of uops a sequence number.

15. (Previously Presented) The apparatus of claim 14, wherein the jump unit is to further store the sequence number of the oldest valid uop in each branch path.

16. (Previously Presented) The apparatus of claim 15, wherein the execution unit is to further compare the sequence number of the uop to the sequence number of the oldest valid uop in the same branch path.

17. (Original) The apparatus of claim 10, further comprising an instruction fetch unit coupled to the allocator to fetch a next instruction based on a next instruction pointer.

18. (Original) The apparatus of claim 17, further comprising an instruction decode unit coupled to the instruction fetch unit to decode the fetched instructions.

19. (Original) A system comprising:
an input/output (I/O) controller; and
a processor coupled to the I/O controller, the processor including:
an allocator to assign micro-operations (uops) identification numbers (IDs), each ID to identify a branch path to which the uop belongs;
a jump unit coupled to the allocator to determine whether branches are predicted correctly; and
an execution unit coupled to the jump unit to determine which uops belong to a branch path that is dependent on a mispredicted branch based on their assigned IDs.

20. (Original) The system of claim 19, wherein the processor further comprises a retire unit coupled to the jump unit to retire uops that are related to a mispredicted branch.

21. (Original) The system of claim 19, wherein the processor further comprises an instruction fetch unit coupled to the allocator to fetch a next instruction based on a next instruction pointer.

22. (Original) The system of claim 21, wherein the processor further comprises an instruction decode unit coupled to the instruction fetch unit to decode the fetched instructions.

EVIDENCE APPENDIX

No evidence is submitted with this appeal.

IX. RELATED PROCEEDINGS APPENDIX

No related proceedings exist.